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PRACTICAL EXPERIENCE:

Montalvo Systems: January 2007-March 31, 2008

- Verification of quadcore 64 bit superscalar "media" processor. Responsible for coherency/switch point: testplan, checker, monitors, and testing. Coherency point involved 4 external interfaces, and 1 internal L3 cache agent. Each agent had multiple virtual channels bound to the interface. Internal data structures included multiple duplicate cache tags (for each virtual channel), victim buffers, 64 deep out-of-order request queue, etc. Wrote random & directed tests in SystemVerilog, AVM, and x86 assembly. Also directed work of contractor and some unofficial tech lead work for junior engineers.

Independent Contractor: *August 2004-Present*

- Team Programming Lead for www.c-loans.com. Managed 4 programmers in addition to active technical contribution. Perl, Postgres, HTML, CSS, and SQL development. Also responsible for system administration, scheduling, client interaction. Roughly $200-300 million (peak around 600 million) per year in closed loans with around $2 million in revenue. Over 160,000 registered "deals" and roughly 500 lenders.
- Wrote Perl code for miscellaneous clients, C/C++ coding, XML parsing/generation, AutoCad file generation. Also modeled RFID reader algorithms in Matlab for startup. Website development & system administration.

AMD: *Design Engineer, October 2005-August 2006 (contractor October-March, site closure Aug 2006)*

- Verification of Wetterhorn x86 core – primarily TLB & Cache. Wrote Test plan, IO/memory checker (in C++ with bison/lex/yacc), tests, and triage/debug failures. Developed templates for x86 assembly tests using gnu assembler. Tech lead of 3 contractors & 5 person software team – assigned work, answered technical questions, reviewed results.

Ball Aerospace: *Contract Verification Engineer, October 2004-May 2005*

- Pioneered "FPGA Verification Methodology". Developed scripts, make/build process, regression testing, checking, formal reviews, random testing, etc. Verified 2 FPGA's in VHDL for Kepler Mission using said methodology. UART, PCI, Bridge, Motor Controller, A2D, and Relay interfaces verified.
- Took on "late" project verification (HiRise/Mars Orbiter) during overtime - SDF & rtl level simulations, and debugging an unknown testbench.

Motorola (C-Port Division): *Design / Verification Engineer, June 2002 – December 2003 (site closure)*

- Designer on the "QX" Quality of Service chips – 150MHz (ASIC) / 100 MHz (FPGA). Delivery block: 512 source to destination mapping. Delivery was based on credits. Developed 8-way Virtual Queuing to target network processor with goal of minimal latency and packet reordering. Also worked on heap sorted list management block.
- Led development of C diagnostic tests for debugging QX FPGA prototype in lab. Assisted with debug of QDR SRAM and clocking for 100MHz operation.
- Responsible for gate level simulations of ASIC including SDF.

Emulex (Giganet Division): *Design/Verification Engineer, September 2000 - June 2002*

- Conceived & led development of performance simulator in C++. Modelled multiple architectures for iSCSI (over TCP/IP) System on a Chip. Simulated BFM's of several embedded ISAs (arm, ppc 405, ppc 440, tensilica), memory controllers, and bus architectures. Wrote event wheel and BFM's of devices. Simulation results used to architect firmware partitioning and hardware acceleration. Used for 2 programs (iSCSI & Fiber Channel)
- Verification of said system: Verilog/C++ based - wrote plans, monitors, GMII/phy models, build process
- Secondary design responsibilities included TX mac interface FIFO development and ECC ram work. System frequency was 125Mhz.

National Semiconductor (Cyrix Division): *Design/Verification Engineer, January 1998 - September 2000*

- Designer Responsible for Instruction Decode and x86 exception units, 2.5ns timing. Added 3DNow!, MMX, and other instructions to instruction decoder. Added performance enhancements to pipe. Redesigned latches to flops and

state machines. Added new suspend modes for lower power. Added additional debug & performance logic.

- Developed Verilog watcher to monitor the integer pipeline and connect to a C++ checker/model. Wrote multiple tests for Pentium/Pentium II class processors. Established template suite for x86 assembly tests. Debugged failing tests in 2500+ test regression suite to root cause & fixed verilog/assembly code.
- Primary Verification engineer responsible for 3d graphics system (8 person DV team - M3D). Wrote testbench, scripts, and bus functional models for processor/memory devices. Prototyped and developed a C++ based testing environment. Similar responsibilities on another project. Wrote SDR & DDR models.
- Verification Tools: Wrote bitwise toggle coverage pli (similar to Covermeter) & backend database. Wrote set of database tools: "diffs" between tests, test suite optimization, power estimation. Spearheaded build & release process for Verilog PLI for 2 sites (400+ people).

Idealogy Inc (now Cadence): *Staff Engineer, May 1997 - December 1997*

- Wrote & maintained verilog models for ATM, SDRAM chips. Wrote an "inverse BNF" random generator in Perl to randomly test software package sold by Idealogy. Developed regression suite of directed and random tests.

University of Colorado Electrical Engineering VLSI Group: *Student Programmer, September 1996 - May 1997*

- Wrote java code to demonstrate VLSI concepts. Provided conceptual design and proof of concept for artificial intelligence "critic/tutor" to provide students with feedback on problem solving.

National Oceanic & Atmospheric Administration: *Staff Programmer, September 1993 - October 1996*

- Programmed data extraction/visualization application in C/C++ & Java as a front end to Oracle. Wrote geophysical data retrieval & plotting system in Tcl/Tk for 2Gb database. Concept & development for 2d color visualization tool to model underwater bathymetry (contour mapping of the sea floor).

EDUCATION: University of Colorado at Boulder, BS Electrical/Computer Engineering
Graduated with Distinction (Cum Laude), December 1997, GPA: 3.77/4.0

PERSONAL INTERESTS:

Rock Climbing, Biking, Fly Fishing, Skiing, Home Theater, Woodworking, Target Shooting, Volunteer work